CLAIMS

What is claimed is:

1. A memory cell comprising:

a thyristor having a cathode and an anode;

an access transistor having one of its source/drain region connected to the cathode of the thyristor; and

a diode having an anode and a cathode, the anode of the diode being connected to the cathode of the thyristor, the cathode of the diode accepting a voltage having a first level at a first time period and a second level at a second time period, with the first level being higher than the second level.

2. The memory cell of claim 1 wherein the second level is equal to approximately zero volt.

3. The memory cell of claim 1 wherein the second level has a negative value.

4. The memory cell of claim wherein the first time period has a duration that is longer than that of the second time period.

5. The memory cell of claim 1 wherein the thyristor comprises a control gate for controlling a conductive state of the thyristor.

6. The memory cell of claim 1 wherein the thyristor performs an internal positive feedback operation during the second time period while in a "1" state.

7. The memory cell of claim 1 wherein the thyristor is a thin capacitively coupled thyristor.

8. A memory array comprising:

at least two sets of memory cells, each set comprising at least a word line, a diode line and at least one memory cell comprising:

a thyristor having a control port and a cathode, the control port being connected to the word line; and

a diode having an anode and a cathode, the anode of the diode being connected to the cathode of the thyristor and the cathode of the diode being connected to the diode line;

the word line and the diode line of the at least two sets being substantially parallel to each other; and

a voltage controller connected to the diode line of at least one of the at least two sets, the voltage controller generating a first level at a first time period and a second level at a second time period, with the first level being higher than the second level.

9. The memory cell of claim 8 wherein the second level is equal to approximately zero volt.

10. The memory cell of claim 8 wherein the second level has a negative value.

11. The memory cell of claim 8 wherein the first time period has a duration that is longer than that of the second time period.

12. The memory cell of claim 8 wherein the thyristor performs an internal positive feedback operation during the second time period while in a "1" state.

13. The memory cell of claim 8 wherein the thyristor is a thin capacitively coupled thyristor.

14. A memory array comprising:

at least two set of memory cells, each set comprising at least a bitline, a diode line and at least one memory cell comprising:

a thyristor having a cathode;

an access transistor having one end connected to the cathode of the thyristor and another end connected to the bit line; and

a diode having an anode and a cathode, the anode of the diode being connected to the cathode of the thyristor and the cathode of the diode being connected to the diode line;

the bit line and the diode line of the at least two sets being substantially parallel to each other; and

a voltage controller connected to the diode line of at least one of the at least two sets, the voltage controller generating a first level at a first time period and a second level at a second time period, with the first level being higher than the second level.

15. The memory cell of claim 14 wherein the second level is equal to approximately zero volt.

16. The memory cell of claim 14 wherein the second level has a negative value.

17. The memory cell of claim 14 wherein the first time period has a duration that is longer than that of the second time period.

18. The memory cell of claim 14 wherein the thyristor performs an internal positive feedback operation during the second time period while in a "1" state.

19. The memory cell of claim 14 wherein the thyristor is a thin capacitively coupled thyristor.